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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,008	10/02/2003	Robert C. Chang	SANDP036	8904

26541 7590 01/18/2006

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EXAMINER
TSAI, SHENG JEN

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/679,008	CHANG ET AL.
	Examiner	Art Unit
	Sheng-Jen Tsai	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.
  4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-42* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  a)☐ All b)☐ Some * c)☐ None of:
    1.☐ Certified copies of the priority documents have been received.
    2.☐ Certified copies of the priority documents have been received in Application No. _____.
    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
  Paper No(s)/Mail Date *10/27/2003*.
4) ☐ Interview Summary (PTO-413)
  Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-42 are presented for examination in this application (10,679,008) filed on October 2, 2003.

Acknowledgement is made to the Information Disclosure Statement received on October 27, 2003.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 8-13, 15-20, 22-26, 28-34 and 36-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Bruce et al. (US 6,000,006).

As to claim 1, Bruce et al. disclose **a method for performing a write operation** [Unified Re-Map and Cache-Index Table with Dual Write-Counters for Wear-Leveling of Non-Volatile Flash RAM Mass Storage (title)] **in a non-volatile memory system** [a flash memory system provides solid-state storage as a replacement to a hard disk (abstract)], **the non-volatile memory system including a non-volatile memory having a memory unit** [NVMEM, figure 4, 24 & 26], **the memory unit being associated with a logical unit** [figures 1-3 show the logical page address], **the memory unit including a first physical sub-unit and a second physical sub-unit** [figures 1-3 shows a plurality of physical pages (i.e., sub-units); for example, physical page 010 may be the first physical sub-unit and physical page 011 may be the second physical sub-unit; other possible pairing of the first and second physical sub-units are obvious], **the second physical sub-unit being sequentially after the memory unit than the first physical sub-unit** [for example, physical page 011 (second sub-unit) is sequentially after physical page 010 (first sub-unit) as indicated by their address in figures 1-3], **the logical unit including a first logical sub-unit and a second logical sub-unit** [figures 1-3 show a plurality of logical pages (i.e., sub-units); for example, logical page 010 may be the first logical sub-unit and logical page 011 may be the second logical sub-unit; other possible pairing of the first and second logical sub-units are obvious], **the second logical sub-unit being sequentially after the first logical sub-unit** [for example, logical page 011 (second sub-unit) is sequentially after logical page 010 (first sub-unit) as indicated by their address in figures 1-3], **the method comprising**:

writing a first set of contents into the first physical sub-unit [an entire block of 16 pages must be erased together, while all 512 bytes on a page must be written together (column 1, lines 21-40)]; **and**

writing a second set of contents into the second physical sub-unit after the first set of contents is written into the first physical sub-unit [an entire block of 16 pages must be erased together, while all 512 bytes on a page must be written together (column 1, lines 21-40)], **wherein the first set of contents is associated with the second logical sub-unit and the second set of contents is associated with the first logical sub-unit** [the re-map table in figures 2-3 shows the association between any two physical pages and the corresponding logical pages].

As to claim 2, Bruce et al. teach that **the first physical sub-unit** [a physical page of 512 bytes (column 1, lines 21-40)] **is a part of a first physical group** [an entire block of 16 pages must be erased together, while all 512 bytes on a page must be written together (column 1, lines 21-40); figures 7A~7E show that contents being erased and written into each of the plurality of blocks, as indicated by the total write counter (TOT_WR'S) and the incremental write counter (INCR_WR'S); column 7, 56-67; column 8, lines 1-67; column 9, lines 1-37] **and the second physical sub-unit is a part of a second physical group** [an entire block of 16 pages must be erased together, while all 512 bytes on a page must be written together (column 1, lines 21-40); figures 7A~7E show that contents being erased and written into each of the plurality of blocks, as indicated by the total write counter (TOT_WR'S) and the incremental write counter (INCR_WR'S); column 7, 56-67; column 8, lines 1-67; column 9, lines 1-37], **the first physical group and the second physical group being associated with the memory unit** [figure 9 shows the association of the physical group to the memory unit (NVMEM, 24 and 26)].

As to claim 3, refer to "As to claim 1" and "As to claim 2." Not that an entire block of 16 pages must be erased together, while all 512 bytes on a page must be written together (column 1, lines 21-40). Figures 7A~7E show that contents being erased and written into each of the plurality of blocks, as indicated by the total write counter (TOT_WR'S) and the incremental write counter (INCR_WR'S). That is, a physical group comprises 16 pages, and each 512-byte page is a sub-unit.

As to claim 4, Bruce et al. teach **writing a first identifier** [the mapping between a physical unit and a logical unit, as shown in figures 2-3; for example, identifier 010 of the re-map table is associated with the first physical unit 010] **into the first physical group** [figure 4 shows that the re-map table be associated with the NVMEMs], **the first identifier being arranged to substantially identify the second logical sub-unit** [the re-map table, figures 2-3]; **and writing a second identifier** [the mapping between a physical unit and a logical unit, as shown in figures 2-3; for example, identifier 011 of the re-map table is associated with the second physical unit 011] **into the second physical group** [figure 4 shows that the re-map table be associated with the NVMEMs], **the second identifier being arranged to substantially identify the first logical sub-unit** [figures 2-3].

As to claim 5, refer to "As to claims 1-4."

As to claim 6, Bruce et al. teach that **the non-volatile memory is a flash memory** [a flash memory system provides solid-state storage as a replacement to a hard disk (abstract)].

As to claim 8, refer to "As to claim 1."

As to claim 9, refer to "As to claim 2."

As to claim 10, refer to "As to claim 4."

As to claim 11, refer to "As to claim 3."

As to claim 12, refer to "As to claim 5."

As to claim 13, refer to "As to claim 6."

As to claim 15, refer to "As to claim 1."

As to claim 16, refer to “As to claim 1.”

As to claim 17, refer to “As to claim 2.”

As to claim 18, refer to “As to claim 3.”

As to claim 19, refer to “As to claim 5.”

As to claim 20, refer to “As to claim 6.”

As to claim 22, refer to “As to claim 1.”

As to claim 23, refer to “As to claim 1.”

As to claim 24, refer to “As to claim 2.”

As to claim 25, refer to “As to claim 3.”

As to claim 26, refer to “As to claim 6.”

As to claim 28, refer to “As to claim 1.”

As to claim 29, refer to “As to claim 3.”

As to claim 30, refer to “As to claim 1.”

As to claim 31, refer to “As to claim 1.”

As to claim 32, refer to “As to claim 1.”

As to claim 33, refer to “As to claim 2.”

As to claim 34, refer to “As to claim 6.”

As to claim 36, refer to “As to claim 1.”

As to claim 37, refer to “As to claim 3.”

As to claim 38, refer to “As to claim 2.” Further, examples are provided to illustrate the re-mapping of first/second physical unit to first/second logical unit as a consequence of wear-leveling operations [column 7, 56-67; column 8, lines 1-67; column 9, lines 1-37].

As to claim 39, refer to "As to claim 2." Further, examples are provided to illustrate the re-mapping of first/second physical unit to first/second logical unit as a consequence of wear-leveling operations [column 7, 56-67; column 8, lines 1-67; column 9, lines 1-37].

As to claim 40, refer to "As to claim 2." Further, examples are provided to illustrate the re-mapping of first/second physical unit to first/second logical unit as a consequence of wear-leveling operations [column 7, 56-67; column 8, lines 1-67; column 9, lines 1-37].

As to claim 41, refer to "As to claim 1."

As to claim 42, Bruce et al. teach that **the code devices are one of software code devices and firmware code devices** [figures 4-6 show the structure of the code devices; the ECC coding scheme may be Hamming code or Reed-Solomon block code that is usually implemented using software (column 9, lines 58-67)].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 7, 14, 21, 27 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bruce et al. (US 6,000,006), and in view of Kramer (US 6,182,239).

As to claims 7, 14, 21, 27 and 35, Bruce et al. do not mention that **the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.**

However, the invention of Bruce et al. is directly applicable to any type of flash memories, including NAND flash memory and MLC NAND flash memory.

Further, Kramer teaches in the invention "Fault-Tolerant Codes for Multi-Level Memories" a fault-tolerant code semiconductor flash memory storage devices including an array of individual multi-level cell (MLC) storage devices [abstract; column 2, lines 1-15] as well as NAND flash memory [column 2, lines 36-57].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to recognize that the particular limitation recited in this claim is well known in the art, as demonstrated Kramer, hence lacking patentable significance.

6. ***Related Prior Art On Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Lofgren et al., (US 6,230,233), "Wear Leveling Techniques for Flash EEPROM Systems."
- Jou et al., (US 5,568,423), "Flash Memory Wear Leveling System Providing Immediate Direct Access to Microprocessor."
- Bruce et al., (US 6,970,890), "Method and Apparatus for Data Recovery."

- Sukegawa et al., (US 5,603,001), "semiconductor Disk System Having a Plurality of Flash Memories."
- Norman, (US 5,754,567), "Write Reduction in Flash Memory systems through ECC Usage."

Conclusion

7. Claims 1-42 are rejected as explained above.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

December 27, 2005

PIERRE BATAILLE
PRIMARY EXAMINER